Where subject matter not shown in the drawing or described in the description is claimed in the application as filed, and such original claim itself constitutes a clear disclosure of this subject matter, then the claim should be treated on its merits, and requirement made to amend the drawing and description to show this subject matter. The claim should not be attacked either by objection or rejection because this subject matter is lacking in the drawing and description. It is the drawing and description that are defective, not the claim.

Applicant also notes that claims 2, 19-20, and 22-23 have at least the following additional support for the elements of claims in the original specification.

In general, claims 2, 19-20, and 22-23 are supported by at least the following: Figs. 1A, 30, 31, 9, 12; Pg. 2, ln. 11-21; Pg. 6, ln. 14-29; Pg. 16, ln. 18 to Pg. 20, ln. 16; Pg. 24, ln. 1-3; Pg. 25, ln. 27 to Pg. 26, ln. 10; Pg. 32, ln.3-13; Pg. 33, ln.9-26; Pg 40, ln. 25 to Pg. 41, ln. 4; Pg. 41, ln. 6-21; Pg. 42, ln. 19 to Pg. 43, ln. 7.

Specifically, the elements of claims 2, 19-20, and 22-23 are supported in the description by at least the following {Claims 1-2, 19-20, and 22-23 are repeated herein for convenience of reference}:

Claim 2

1. A method of writing to a synchronous non-volatile memory device comprising:
receiving write data on a first clock cycle and executing a data write operation; and
executing a data read operation on a next clock cycle immediately following the first clock cycle.

2. The method of claim 1 wherein the data write operation is executed on a first memory bank of the synchronous non-volatile memory device and the data read operation is executed on a second memory bank.

Element (Support)

Claim 2 – Pg. 25, ln. 27 to Pg. 26, ln. 10; Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Pg. 40, ln. 25 to Pg. 41, ln. 4; Fig. 30; Fig. 31; Pg. 41, ln. 6-21; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Pg. 16, ln. 18 to Pg. 20, ln. 16.

Claims 19 & 20

19. A method of operating a synchronous memory device comprising:

receiving a read command and corresponding column address on a first clock cycle to request output data from a memory array of the synchronous memory, wherein the output data is provided on an external data connection a predefined number of clock cycles following the first clock cycle; and

receiving a first command of a write command sequence on a second clock cycle immediately following the first clock cycle to initiate a write operation to the memory array such that the write command is provided in coincidence with or prior to providing the output data on the external data connection.

20. The method of claim 19 wherein the write command sequence comprises:

a load command register cycle used to initiate the write operation;

an active cycle used to define and activate a selected row of the memory array; and

a write cycle used to define a column of the memory array and provide write data on the external data connection.

Element (Support)

Claim 19 – Pg. 42, ln. 19 to Pg. 43, ln. 7; Fig. 9; Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Pg. 25, ln. 27 to Pg. 26, ln. 10; Pg. 16, ln. 18 to Pg. 20, ln. 16; and Pg. 2, ln. 11-21.

Claim 20 – Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Truth Table 2; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Pg. 16, ln. 18 to Pg. 20, ln. 16.

Claims 22-23

22. A method of initiating a write operation in a memory system, the method comprises:

providing a read command from a processor to a synchronous memory device;

providing a memory array address from the processor to the synchronous memory device on a first clock cycle of a memory array location to perform a read operation;

providing a first command of a write command sequence from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a write operation of the memory array such that the write command is provided prior to providing output data from the memory array address on an external data connection.

23. The method of claim 22 wherein the write command sequence comprises:

a load command register cycle used to initiate the write operation;

an active cycle used to define and activate a selected row of the memory array; and

a write cycle used to define a column of the memory array and provide write data on the external data connection.

Element (Support)

Claim 22 – Pg. 32, ln. 3-13; Fig. 9; Truth Table 2; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Pg. 16, ln. 18 to Pg. 20, ln. 16.

Claim 23 – Pg. 32, ln. 3-13; Pg. 33, ln. 9-26; Pg. 42, ln. 19 to Pg. 43, ln. 7; and Truth Table 2.

Applicant respectfully requests that the rejection of the claims 2, 19-20, and 22-23 be withdrawn in light of the above arguments and that the specification does clearly describe the invention in a way to enable one skilled in the art to make or use the invention.

Claim Rejections Under 35 U.S.C. § 102

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but identical terminology is not required. *In re Bond,* 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.,* 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.,* 75 F.3d 1558, 37 U.S.P.Q.2d 1618 (Fed. Cir. 1996).

Each of the claims 1-27 contain elements or limitations not present in the cited art, and as such, the rejections discussed below under 35 U.S.C. § 102 are improper and not supported.

Claims 1-13 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Cowles et al. (U.S. Patent 5,263,003).

Applicant respectfully disagrees with the Examiner and traverses this rejection, requesting reconsideration of the claims. Applicant feels that claims 1-13 are allowable for the following reasons.

In the Office Actions dated August 20, 2002 and January 24, 2003, the Examiner stated that Figures 1-3 of Cowles et al. detail a synchronous flash memory system citing lines 24-27 of column 5 of Cowles et al. In these Office Actions and in the telephonic interview with the Applicant on March 19, 2003 the Examiner stated that because Cowles et al. details a system that contains a serial I/O (SIO) communication controller 44 which services two synchronous communication channels, a clock circuit 60, a system

controller 61, and a Flash memory 55 that the system is inherently a synchronous non-volatile Flash memory system, regardless of the type of Flash memory that is coupled to the system.

The Applicant strongly disagrees with the assertion that a system containing a synchronous component means that the memory of the system is inherently synchronous and cites Barth et al. (U.S. Patent 6,532,522, Titled: "Asynchronous request/synchronous data dynamic random access memory", Issued: March 11, 2003) to refute the Examiner's argument of inherency:

> In conventional memory systems, the communication between a memory controller and DRAMs is performed through asynchronous communications. For example, the memory controller uses control signals to indicate to the DRAM when requests for data transactions are sent. The data transfers themselves are also performed asynchronously. To meet increased speed requirements, various enhanced asynchronous memory systems have been developed. One such system is the Extended Data Out (EDO) DRAM memory system.
>
> FIG. 1 is a block diagram illustrating a typical EDO DRAM system 100. In the EDO DRAM system 100, data transfers are performed asynchronously in response to control signals and addresses sent from pin buffers 116 of a memory controller to pin buffers 118 of the EDO DRAM over a plurality of lines 120, 122, 124, 134, and 136. Specifically, lines 122 carry an address that is stored in latches 112 and 114. Line 120 carries a row address strobe (RAS) that controls when the address stored in latch 112 is sent to row decoder 106. Line 136 carries a write enable signal that controls timing chains 108 and the direction of data flow on the bi-directional data bus 126.
>
> ...
>
> DRAMs built with an asynchronous RAS/CAS interface have difficulty meeting the high memory bandwidth demands of many current computer systems. As a result, synchronous interface standards have been proposed. These alternative interface standards include Synchronous DRAMs (SDRAMs). In contrast to the asynchronous interface of EDO DRAMS, SDRAM systems use a clock to synchronize the communication between the memory controller and the SDRAMs. Timing communication with a clock allows data to be placed on the DRAM output with more precise timing. In addition, the clock signal can be used for internal pipelining. These characteristics of synchronous communication results in higher possible transfer rates.
>
> FIG. 3 is a block diagram illustrating a conventional SDRAM system 300. In system 300, the memory controller includes a plurality of clocked buffers 304 and the SDRAM includes a plurality of clocked buffers 306. Data from control line 310 and an address bus 312 are received by a finite state machine 308 in the SDRAM. The output of the finite state machine 308 and the address data are sent to memory array 302 to initiate a data transfer operation.
>
> FIG. 4 is a timing diagram that illustrates the signals generated in system 300 during a read operation. At time T0 the memory controller places a read

request on line 310 and an address on bus 312. At time T1 the SDRAM reads the information on lines 310 and 312. Between T1 and T2 the SDRAM retrieves the data located at the specified address from memory array 302. At time T2 the SDRAM places data from the specified address on data bus 314. At time T3 the memory controller reads the data off the data bus 314.

Because system 300 is synchronous, various issues arise that do not arise in asynchronous systems. Specifically, the synchronous system has numerous pipeline stages. Unbalanced pipeline stages waste computational time. For example, if a shorter pipeline stage is fed by a longer pipeline stage, there will be some period of time in which the shorter pipeline stage remains idle after finishing its operation and before receiving the next set of data from the preceding pipeline stage. Similarly, if a short pipeline stage feeds a longer pipeline stage, the shorter pipeline stage must wait until the longer pipeline stage has completed before feeding the longer pipeline stage with new input.

See, e.g., Barth et al., column 1, lines 21-46, column 2, line 48 to column 3, line 3, and Figures 1, 2, 3 and 4. Applicant further asserts that the difference between asynchronous memory types (ROM, DRAM, EEPROM, Flash, and SRAM, etc.) with an asynchronous memory interface and synchronous memory types (SDRAM, DDR, etc.) is well known in the art. As such, Applicant submits that Cowles et al. does not teach or describe a system with a synchronous non-volatile Flash memory.

Applicant also notes that Cowles et al. is directed to a memory controller and a flash memory system having multiple individual flash memory devices and not a synchronous non-volatile memory device.

The Examiner further stated that in Cowles et al. the write cycle immediately followed a read cycle, citing lines 40-62 of column 7. The Applicant disagrees and asserts that column 7, lines 40-62 describe a burst addressing mode of multiple consecutive reads or multiple consecutive writes utilizing the addressing mode ability of the underlying Flash memory devices and does not teach or disclose a write cycle immediately followed by a read cycle. The Applicant also notes that Cowles et al. discloses that only an entire memory bank can be reprogrammed (written) at once after it has been through an erasure cycle. Applicant asserts that this mandatory erasure cycle before writing eliminates the possibility of a write immediately following a read cycle. See e.g., Cowles et al., column 13, lines 38-50. As such, with the burst addressing mode and the mandatory erasure before reprogramming of an entire memory bank at once, the

Applicant submits that Cowles et al. does not teach or disclose a write cycle immediately following a read cycle.

In addition, the Applicant notes that the memory banks 71 and 72 cited by the Examiner in Cowles et al. disclose memory banks comprised of individual Flash memory devices and as such do not occur within a single Flash memory device as disclosed by the Applicant's specification. As such, Cowles et al. does not teach or disclose an individual synchronous Flash memory device.

The Examiner further stated that in Cowles et al. duplicate copies of data in the Flash memory 55 can be updated/latched/hold, citing lines 13-21 of column 12. Applicant disagrees and asserts that column 12, lines 13-21 describe storing a duplicate copy of Flash memory system operating routines (that contain the software drivers for operating the Flash memory system and the individual Flash memory devices it contains) in the unselected bank of Flash memory devices while the selected bank of Flash memory devices is erased and reprogrammed, so that they are backed up and not lost. Applicant submits that these are duplicate copies of data already stored in the Flash memory system and not data currently being written/read from the Flash memory system. Additionally, these are not latches but Flash memory devices and that the data is held in the Flash memory arrays of the Flash memory devices. Also, that the elements cited by the Examiner are multiple Flash memory devices and not latches within a single Flash memory device. Further, as stated above, this functionality backs up the software driver routines for the Flash memory so that they are not lost during reprogramming. As such, with the cited elements being Flash Memory devices and not latches, the data being held having already been written/stored in the Flash memory system, and it not being an individual Flash memory device, that Cowles et al. does not teach or disclose a latch for latching write data as used and recited in the Applicant's claims.

Applicant respectfully submits that Cowles et al. does not teach or suggest a method of writing to a synchronous non-volatile memory device by receiving write data on a first clock cycle and executing a data write operation and executing a data read operation on a next clock cycle immediately following the first clock cycle.

As such, since Cowles et al. does not describe a synchronous non-volatile/Flash memory device, Cowles et al. does describe memory banks with multiple individual Flash memory devices, no write cycle immediately following a read is present, and write data latches are not present, each and every limitation of the claims 1-13 are not present in Cowles et al., and the rejection is improper. Claims 1-13 are allowable.

Applicant respectfully contends that claims 1-13 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant requests reconsideration and withdrawal of the final rejection under 35 U.S.C. § 102(b) and allowance of claims 1-13.

Claims 14-27 were rejected under 35 U.S.C. § 102 (b) as being anticipated by Patel (U.S. Patent 5,539,696).

Applicant respectfully traverses this rejection and requests reconsideration of the claims. Applicant feels that claims 14-27 are allowable for the following reasons.

In the Office Actions dated August 20, 2002 and January 24, 2003, the Examiner stated that Figure 1 details a synchronous memory system 10 which can be used with nonvolatile EEPROM, PROM, or ROM devices citing lines 22-25 of column 4 of Patel. In these Office Actions and in the telephonic interview with the Applicant on March 19, 2003 the Examiner stated that because Patel details a system that contains a SDRAM cell array 14 but also with non-volatile EEPROM devices that the system is inherently a synchronous non-volatile memory system, regardless of the type of non-volatile memory that is couple to the system.

Applicant submits that Patel teaches a synchronous memory device that allows faster burst data write operations by using parallel latches of the input buffers, see column 5, line 64 to column 6, line 26. The banks of the memory array are divided into column independent sections that are simultaneously written to from the buffer parallel latches.

The Applicant, as above, strongly disagrees with the assertion that a system containing a synchronous component means that all memory of the system is inherently synchronous and cites Barth et al. column 1, lines 21-46, column 2, line 48 to column 3, line 3, and Figures 1, 2, 3 and 4, as above. Applicant also asserts that Patel discloses an

asynchronous EEPROM and that the mere description of an invention that can be used with an SDRAM and other types of memory (EEPROM) does not teach or suggest or enable one skilled in the art to practice the disclosed invention of Patel with synchronous non-volatile memory devices or practice synchronous non-volatile memory in general. As such, Applicant submits that Patel does not teach or describe the element of a system with a synchronous non-volatile/Flash memory.

The Examiner also stated that Patel disclosed a synchronous memory that included write latches 110 and 102, 104, 106, and 108, as shown in Figure 3. The Examiner further stated that synchronous memory cell array 14 and write latches 102-110 are coupled to the input/output data buffer circuit I/O 26 of Figure 1.

Applicant disagrees and asserts that Figure 3 of Patel teaches a latch circuit 100 that contains latches 102, 104, 106, and 108 and a write latch control circuit 110 wherein the write control circuit which latch to receive data for its coupled array bank in combination with the column address and does not teach or disclose a write latch where the write latch may be coupled to any memory bank. *See, e.g.,* Patel, column 11, lines 31-38. In addition, Applicant also asserts that Figure 1 of Patel teaches a separate synchronous peripheral I/O device 26 coupled to a digital processor 12 and a input/output data buffer circuit I/O of a synchronous memory device. *See, e.g.,* Patel, column 4, lines 31-37. As such, Patel does not teach or suggest a system having a synchronous non-volatile memory wherein the synchronous memory has an input/output data buffer coupled to a write data latch.

Applicant therefore respectfully submits that Patel does not teach or suggest a memory system having a processor and a synchronous memory device coupled to the processor via a bi-directional data bus. The synchronous memory device comprising a memory array arranged in rows and columns, data communication connections coupled to the bi-directional data bus, an input/output data buffer coupled to the data communication connections to manage bi-directional data communication, and a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections.

Applicant also notes that the presence of synchronous dynamic memory devices that can be written or read in a burst mode does not preempt the present invention or

make it obvious. There is no discussion in Patel of the timing between write and read operations. It is well known in the synchronous dynamic memory art that there is a minimum time (such as write recovery and precharge times) that prohibit read operations from immediately following a write operation.

As such, since Patel does not describe a synchronous non-volatile/Flash memory device, write latches where the write latches may be coupled to any memory bank are not present, the cited I/O buffer 26 is not internal to the memory device, and that a write following a read is not disclosed that each and every limitation of the claims 14-27 are not present in Patel, and the rejection is improper. Claims 14-27 are allowable.

Applicant respectfully contends that claims 14-27 have been shown to be patentably distinct from the cited reference. Accordingly, Applicant requests reconsideration and withdrawal of the final rejection under 35 U.S.C. § 102(b) and allowance of claims 14-27.

CONCLUSION

Applicant believes that the claims are in condition for allowance and respectfully requests a withdrawal of the Final Rejection and a Notice of Allowance be issued in this case. If the Examiner has any questions regarding this application, please contact the under-signed at (612) 312-2207.

Respectfully submitted,

Date: 3/24/03

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